CLAIMS

What is claimed is:

1. An electronics interface for interfacing to a multi-channel photo array comprising a plurality of parallel channels, each one of the parallel channels outputting a photo detector signal corresponding to a different image depth, the electronics interface comprising:

a plurality of channel processors, each one of the channel processors having an input coupled to one of the parallel channels of the photo array to permit each one of the channel processors to acquire the photo detector signal from the respective parallel channel, each one of the channel processors further having an output;

a data bus coupled to the output of each one of the channel processors; and

a memory buffer having an input coupled to the data bus and an output.

2. The electronics interface of claim 1, wherein the memory buffer is a First-In-First-Out (FIFO) memory buffer.

3. The electronics interface of claim 1, wherein the memory buffer outputs data in the form of a digital data sequence arranged in order of increasing image depth.

4. The electronics interface of claim 1, wherein the memory buffer outputs data in the form of a digital data sequence arranged in order of decreasing image depth.

5. The electronics interface of claim 1, wherein each one of the channel processors comprises:

an analog processor having an input coupled to one of the parallel channels of the photo array, and an output;

an analog-to-digital converter having an input coupled to the output of the analog processor, and an output; and

a memory buffer having an input coupled to the output of the analog-to-digital converter and an output coupled to the data bus.

6. The electronics interface of claim 5, wherein the memory buffer of each one of the channel processors is a First-In-First-Out memory buffer.

7. The electronics interface of claim 1 further comprising a digital-to-analog converter having an input coupled to the output of the memory buffer, and an output.

8. The electronics interface of claim 1 wherein the output of the memory buffer outputs digital data to an ultrasound console.

9. The electronics interface of claim 7, wherein the output of the digital-to-analog converter is coupled to provide a serial analog signal to an ultrasound console.

10. The electronics interface of claim 7, wherein the output of the digital-to-analog converter is coupled to a mixer.

11. The electronics interface of claim 7, wherein the memory buffer outputs digital data received from the channel processors to the digital-to-analog converter in the form of a digital data sequence.

12. The electronics interface of claim 11, wherein the digital data in the digital data sequence are arranged in order of increasing image depth.

13. The electronics interface of claim 11, wherein the digital data in the digital data sequence are arranged in order of decreasing image depth.

14. The electronics interface of claim 1 further comprising a controller coupled to an ultrasound motor encoder for synchronizing the electronics interface with an ultrasound console.

15. The electronics interface of claim 14, wherein the controller instructs each one of the channel processors to acquire digital data from the respective parallel channel for a predetermined data acquisition period when the controller receives an encoder pulse from the ultrasound motor encoder

16. The electronics interface of claim 15, wherein the channel processors write their digital data into the memory buffer at the end of the data acquisition period.

17. The electronics interface of claim 16 further comprising a digital-to-analog converter having an input coupled to the output of the memory buffer and an output coupled to the ultrasound console.

18. The electronics interface of claim 17, wherein the controller instructs the memory buffer to output the digital data received from the channel processors to the digital-to-analog converter when the controller receives a subsequent encoder pulse from the ultrasound motor encoder.

19. The electronics interface of claim 16, wherein the memory buffer outputs the digital data in the form of a digital data sequence to an ultrasound console.

20. The electronics interface of claim 19, wherein the digital data in the digital data sequence are arranged in order of increasing image depth.

21. The electronics interface of claim 19, wherein the digital data in the digital data sequence are arranged in order of decreasing image depth.

22. The electronics interface of claim 19, wherein the digital-to-analog converter converts the received digital data into an analog signal and outputs the analog signal to the ultrasound console.

23. The electronics interface of claim 22, wherein the digital-to-analog converter outputs the analog signal to the ultrasound console in the form of a serial analog signal.

24. The electronics interface of claim 16, further comprising a logic control having an input coupled to the memory buffer and an output coupled to a digital input of the ultrasound console.

25. The electronics interface of claim 24, wherein the controller instructs the logic control to transfer the digital data stored in the memory buffer to the ultrasound console when the controller receives a subsequent encoder pulse from the ultrasound motor encoder.

26. The electronics interface of claim 25, wherein the control logic transfers the digital data to the ultrasound console in form of a digital data sequence.

27. The electronics interface of claim 26, wherein the digital data in the digital data sequence are arranged in order of increasing image depth.

28. An electronics interface for interfacing to a multiplexed photo array comprising at least one channel output, each one of the channel outputs capable of outputting a signal from each one of a plurality of photo detectors, each one of the plurality of photo detectors corresponding to a different image depth, the electronics interface comprising:

at least one channel processor, each one of the channel processors having an input coupled to one of the channel outputs of the multiplexed photo array and an output, wherein each one of the channel processors acquires digital data from the respective channel output;

a data bus coupled to the output of each one of the channel processors; and

a memory buffer having an input coupled to the data bus and an output.

29. The electronics interface of claim 28, wherein the multiplexed photo array comprises exactly one channel output.

30. The electronics interface of claim 28, wherein the multiplexed photo array comprises exactly two channel outputs.

31. The electronics interface of claim 28, further comprising a digital-to-analog converter having an input coupled to the output of the memory buffer and an output.

32. The electronics interface of claim 31, wherein the output of the digital-to-analog converter is coupled to an ultrasound console.

33. The electronics interface of claim 28, further comprising a controller coupled to an ultrasound motor encoder for synchronizing the electronics interface and the multiplexed photo array with an ultrasound console.

34. The electronics interface of claim 33, the controller instructs each one of the channel outputs of the multiplexed photo array to sequentially output the signal from each one of its respective plurality of photo detectors when the controller receives an encoder pulse from the ultrasound motor encoder.

35. The electronics interface of claim 34, wherein the controller coordinates the timing of the channel outputs of the photo array and the channel processors such that each one of the channel processors acquires at least one digital datum for each photo detector signal outputted by the respective channel output.

36. The electronics interface of claim 35, wherein each one of the channel processors writes its digital data into the memory buffer via the data bus.

37. The electronics interface of claim 36, further comprising a digital-to-analog converter having an input coupled to the output of the memory buffer and an output coupled to the ultrasound console.

38. The electronics interface of claim 37, wherein the controller instructs the memory buffer to output the digital data received from the channel processors to the digital-to-analog converter when the controller receives a subsequent encoder pulse from the ultrasound motor encoder.

39. The electronics interface of claim 38, wherein the memory buffer outputs the digital data to the digital-to-analog converter in the form of a digital data sequence.

40. The electronics interface of claim 39, wherein the digital data in the digital data sequence are arranged in order of increasing image depth.

41. The electronics interface of claim 39, wherein the digital-to-analog converter converts the received digital data into an analog signal and outputs the analog signal to the ultrasound console.

42. The electronics interface of claim 41, wherein the digital-to-analog converter outputs the analog signal to the ultrasound console in the form of a serial analog signal.

43. The electronics interface of claim 36, further comprising a logic control having an input coupled to the memory buffer and an output coupled to a digital input of the ultrasound console.

44. The electronics interface of claim 43, wherein the controller instructs the logic control to transfer the digital data stored in the memory buffer to the ultrasound console when the controller receives a subsequent encoder pulse from the ultrasound motor encoder.

45. The electronics interface of claim 44, wherein the control logic transfers the digital data to the ultrasound console in form of a digital data sequence.

46. The electronics interface of claim 45, wherein the digital data in the digital data sequence are arranged in order of increasing image depth.